

Broadband Microwave Hybrid Distributed Amplifier on Silicon Wafer

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Abstract— A broadband hybrid distributed amplifier is realized up to 12 GHz frequency range. This investigation in hybrid form on 375 μm thick high resistivity silicon substrate with 50 Ω input and output coplanar lines is considered as pre step for quasi monolithic technology. Silicon technology is mature; both for production of the uniformly polished high purity substrates and for device fabrication and integration. High resistivity silicon offers constant thickness and high dielectric constant, which is stable with frequency. In this approach, commercial 0.25 μm PHEMTs are used for amplifier fabrication. Computer simulations and experimental results are presented.

Keywords: Distributed Amplifier, Hybrid, Broadband, Coplanar, Silicon.

I. INTRODUCTION

The performance of distributed amplifiers has been demonstrated in several investigations. The wide bandwidth capability of such amplifiers is well known [1-2]. Such types of amplifiers are very attractive for high speed optoelectronic and communication applications [3-4]. In this paper, a small signal hybrid distributed amplifier is presented where the active devices are combined with coplanar transmission lines on silicon substrate (Fig. 1). This preliminary design demonstrates the feasibility of a hybrid distributed amplifier with coplanar lines on high resistivity silicon substrate. This realization can be considered as a pre-step to the multistage quasi monolithic integration method described in [5 - 7].

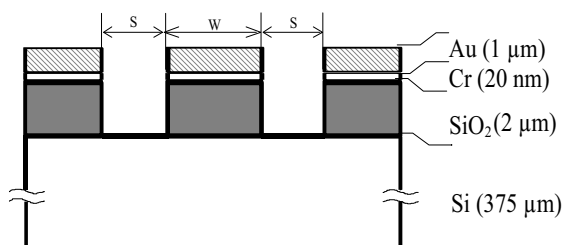


Fig. 1: Coplanar line on Silicon substrate
(Resistivity = 5 k $\Omega\cdot\text{cm}$, $\epsilon_r = 11.9$)

II. THIN FILM TECHNOLOGY

At first, we have the a 375 μm silicon wafer which will be prepared for circuit realization. The thin film technology [8] consists to place a thin film material on a wafer through the evaporation of the material from a hot source. The evaporation system uses a vacuum chamber which is pumped down to 10^{-6} Torr. In the first step a 2 μm silicon-dioxide SiO_2 layer is grown using wet and dry thermal oxidation. Than a thin film of Chrome Cr (20 nm) is deposited using evaporation. This second layer is important for good metal adhesion. The next step is the metallization which consists to evaporate a 2 μm of Gold Au layer. At this point the silicon surface is prepared for amplifier circuit realization. The layout of the circuit is transferred on the substrate using a mask fabrication and Photolithography as shown in Fig. 2.



Fig. 2: Photo of the realized layout (2.8 cm x 1.4 cm) of the distributed amplifier on quarter silicon wafer

I. DESIGN OF THE AMPLIFIER

The topology of the amplifier is shown in Fig. 3. The amplifier consists of four 0.25 μm pHEMTs. The design is based on accurate extraction of 15 element small signal equivalent circuit model of the FET [9]. The difference between phase velocity of gate and drain lines which is due to the difference of the input and output capacitance of the FETs is compensated by adding a short coplanar line (l_{dd}) between the drain lines and each FET leading to equal length of gate and drain line sections (l_g, l_d). The terminations resistances are optimized towards best input and output reflections and gain flatness. The predicted performance of the amplifier is 1 to 12 GHz with 12 dB ± 0.5 dB gain. First, the amplifier was simulated with analytically calculated lumped equivalent circuit of the line in MDS [10], then the length of lines was derived from the comparison of the simulation data between the simple model as an equivalent lumped elements circuit of the coplanar line (Fig. 4) and the MDS-coplanar line model (Fig. 5). The comparison gives very good compatibility up to 28 GHz for the magnitude (Fig. 6) and a good phase approximation up to 40 GHz (Fig. 7). In this case, the optimized length of the lines sections are $l_g = l_d = 1.1872$ mm and $l_{dd} = 0.6547$ mm.

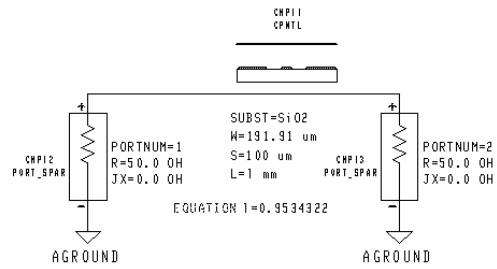


Fig. 5: MDS coplanar line

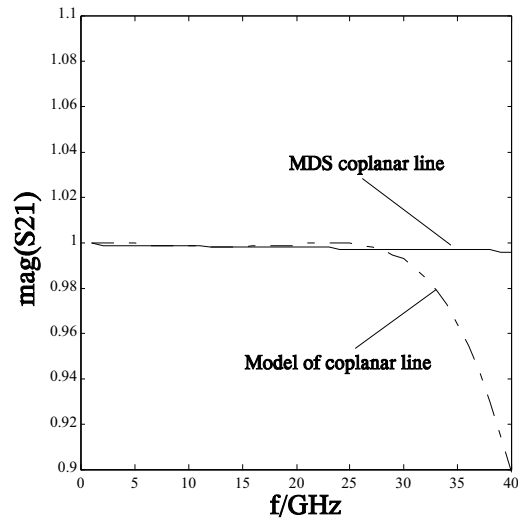


Fig. 6: Magnitude of the transmission coefficient of the coplanar line

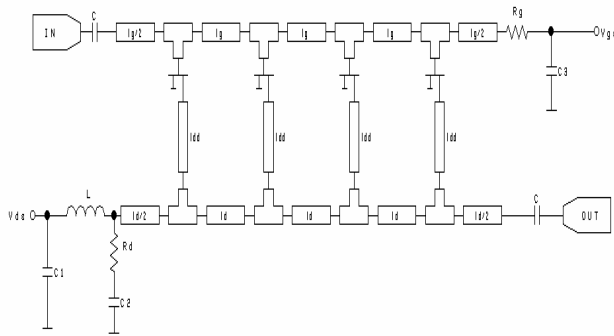


Fig. 3: Topology of the distributed amplifier

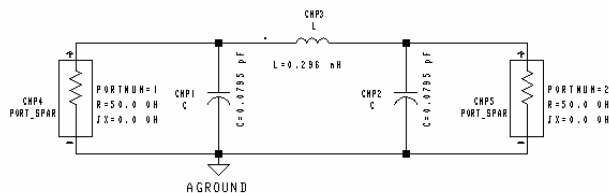


Fig. 4: Lossless lumped elements model of the coplanar line

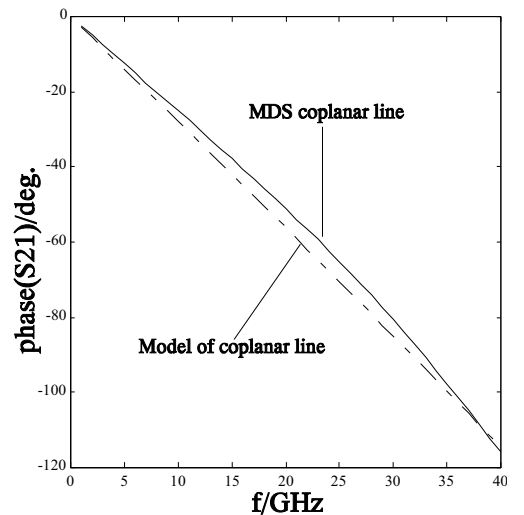


Fig. 7: Phase of the transmission coefficient of the coplanar line

II. AMPLIFIER CIRCUIT REALIZATION

Fig. 8 illustrates the CAD coplanar layout of the distributed amplifier. The amplifier is optimized with MDS for four stages and realized on the silicon wafer as presented in the photo of Fig. 2 using a bond & wire hybrid coplanar technology. The active and the passive devices are first fixed on the silicon substrate using adequate double component glue. The used transistors are four low noise GaAs-pHEMT-chips bonded to the coplanar circuit with 17 μm diameter gold wire. The passive elements are soldered to the coplanar-lines.

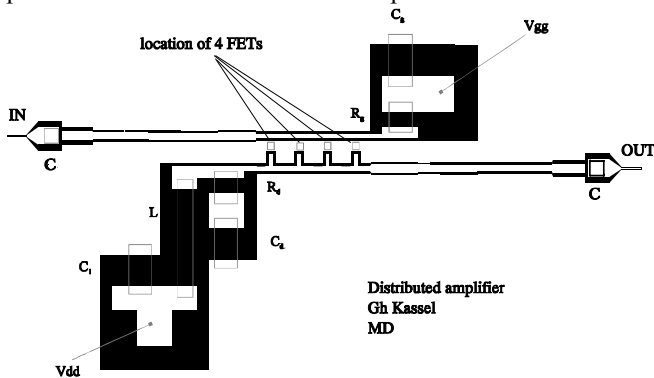


Fig. 8: Layout of the distributed amplifier on Silicon substrate

III. EXPERIMENTAL RESULTS

On-wafer bias-dependent S-parameter measurements (0.1- 15 GHz) for the amplifier have been made using an HP 8510B network analyzer. Figs. 9 to 12 present the measured S-parameter for the bias point $V_{ds} = 2\text{ V}$ and $V_{gs} = 0.6\text{ V}$. The predicted bandwidth has been attained; the gain is 2 dB lower than that simulated. The input and output reflection coefficients are less than -5 dB showing some discrepancies relative to those simulated due to the mismatching of the load impedances. However there is good agreement between the measured and simulated Isolation (22 dB).

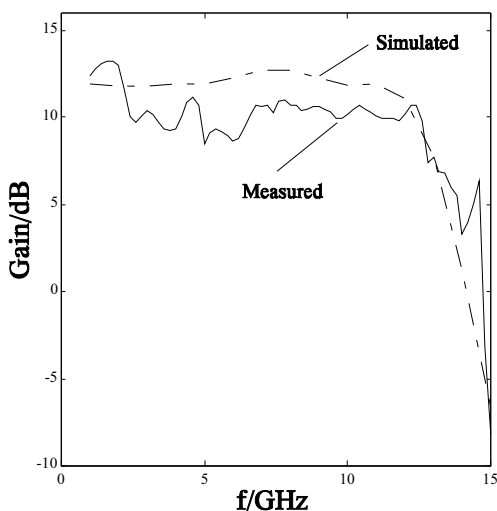


Fig. 9: Gain of the distributed amplifier

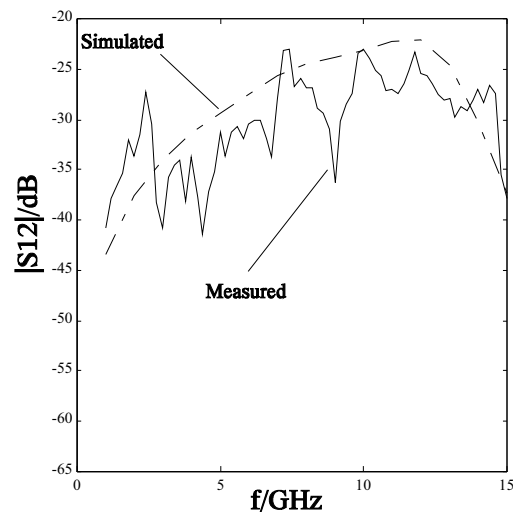


Fig. 10: Isolation of the distributed amplifier

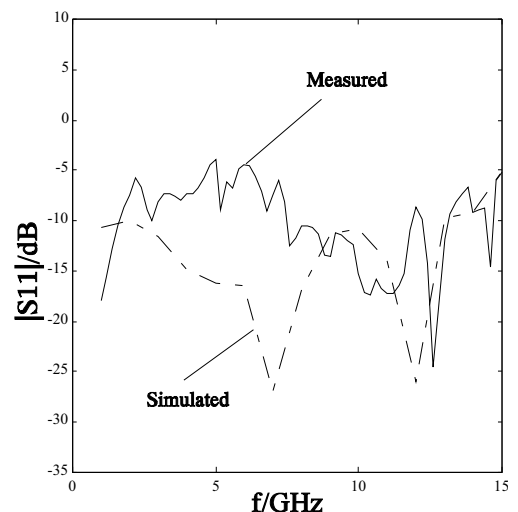


Fig. 11: Input Reflection Coefficient

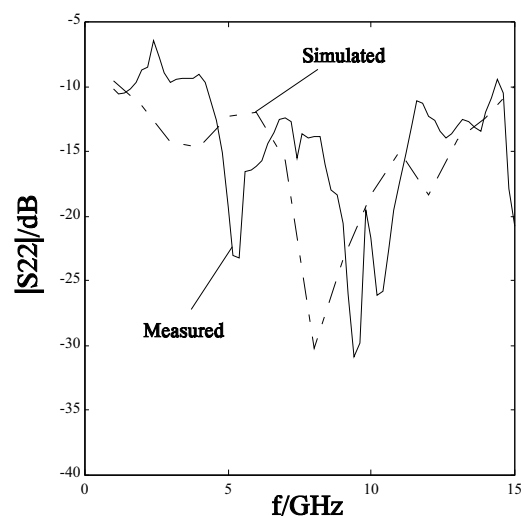


Fig. 12: Output Reflection Coefficient

IV. CONCLUSION

A hybrid distributed amplifier in the band range 1 to 12 GHz using coplanar transmission lines on high resistivity silicon substrate is realized. The silicon wafer is prepared for the amplifier plantation using the thin film technology. A very simple amplifier structure has been demonstrated. The amplifier achieved 10 ± 2 dB gain, an input and output reflection coefficient less than -4 dB and an isolation coefficient less than -22 dB. The ripple can be reduced using better parasitic elements handling and better matching of the bias circuitry. The bonding of active devices to the passive circuit causes parasitic effects which produce mismatching in the amplifier. This amplifier investigation on silicon is considerate as a pre step for a multistage amplifier quasi monolithic from technology on silicon.

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